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Please replace the paragraph beginning at line 22 on page 13 with the following clean replacement paragraph in accordance with 37 CFR § 1.121(b)(1)(ii). A marked-up version showing amendments to the specification paragraph being changed is provided in one or more accompanying pages separate from this amendment in accordance with 37 CFR § 1.121(b)(1)(iii).

Sub B2

Another implementation is described with reference to Figs. 6-7. Like numerals from the first-described embodiment are utilized where appropriate, with differences being indicated with the suffix "b" or with different numerals. Fig. 6 is a sectional view or cut corresponding to that of Fig. 2, and depicts processing occurring subsequent to that of Fig. 2. Accordingly, an array 10b in accordance with this particular preferred embodiment is processed initially to the point as depicted in Fig. 2 in the first-described embodiment. A series of alternating trench isolation regions 22 and active areas 18 are thereby provided within semiconductor substrate 11 in a line adjacent and along at least a portion of lines of floating gates 12 and 14. Such defines a series of discrete transistor source areas separated by trench isolation regions. Floating gate word line patterning thereafter occurs, followed by drain region formation as described above. Lines of floating gates 12 and 14 as depicted in Fig. 7 (as well as in Figs. 8 and 9 described subsequently) comprise a gate dielectric layer, floating gate regions 23 formed thereover, an interpoly dielectric layer formed over floating gate regions 23, a conductively doped polysilicon/silicide stack formed over the interpoly dielectric layer, and an insulative cap formed over the conductively doped polysilicon/silicide stack.

A1